2.4 A 0.1mm², Digitally Programmable Nerve Stimulation Pad Cell with High-Voltage Capability for a Retinal Implant

M. Ortmanns[1], N. Unger[1], A. Rocke[1], M. Gehrke[2], H.J. Tietdke[2]

[1]sci-worx, Hannover, Germany
[2]IIP Technologies, Bonn, Germany

Functional electrical stimulation of the retina has received increasing attention over the last several years [1][2]. It restores basic vision through electrical nerve stimulation within the eyeball of blind people with retina degeneration. The system, known as an epiretinal prosthesis, is shown in Fig. 2.4.1.

Electrical stimulation generates a nerve reaction upon the transfer of charge into the tissue via electrodes. For a retinal stimulator the integration of several hundreds of such stimulation sites is required in order to restore basic vision functions [1][3]. Reliable operation of a nerve stimulator demands high ESD robustness at the electrodes. In addition, electrolysis caused by excess dc-current flow must be safely prevented, since it yields electrode and tissue destruction. The electrode impedance Re (Fig. 2.4.1) depends on the electrode size. For the retinal implant it is typically >10kΩ. This requires high voltage (HV) swing capabilities at the stimulation electrodes for feasible stimulation currents of up to 1mA [3]. Concurrently, the implanted system must be low power and the possible chip size is limited.

Recent implementations of retina stimulators have focused on an increasing number of stimulation sites, and more than 100 have been achieved [1][2]. Common architectures use global generation of stimulation currents and distribution over current switches, which allows only one single or a small number of electrodes to be activated at a time. Besides the usage of biphasic current pulses [1], charge balancing is either not covered [2] or implemented passively with electrode shorting resistors [3]. This is either power-ineffective, when permanently shorted, or requires switches to short only after stimulation. Moreover, ESD protection has not been addressed in recent publications, but it is of major concern due to the very large number of open contacts during surgery. Finally, the possible stimulation current is mostly limited by the output voltage swing capabilities; even with electrode reversal, only ±7V has been achieved [3].

This design presents the concept of an array of fully digitally interfaced and programmable stimulation pad cells for a retinal implant in 0.35µm HVCMOS, which features a maximum voltage swing of ±15V, includes full custom ESD protection and an innovative active charge balancer [4]. Global functions (CDR, supply, ADC, controller, test) are shared. All local stimulation functions are concentrated in each stimulation pad cell. These pads are programmable over a bus by the global controller. The local functions include a 5b current steering DAC with 2 bias points and an output range of 0.8µA-32µA or 3.2µA-99.2µA. The DAC current is fed into a push-pull output current source (OCS), where a gain of 5 or 10 can be adjusted. This yields a stimulation current between 4µA and 992µA (DR≈50dB). The output node features custom ESD protection, HV swing capability and both polarities enabling biphasic, coarsely charge-balanced pulses. To account for biphasic pulse mismatch, an active design for a charge balancer is proposed. Besides, a resistive voltage divider with S/H circuit can sample the electrode voltage, which is then provided to one global ADC. A local digital control is implemented in each pad, which is the interface to the bus and operates all local functionality. A block diagram of the system and the pad cell is shown in Fig. 2.4.2.

This architecture allows serial global acquisition of stimulation data, local programming and then parallel activation of a single, several or even all implemented pad cells of the complete implant with different local stimulation amplitudes and polarities. A layout of the pad cell is shown in Fig. 2.4.3. It only requires a die area of 0.1mm² and consumes less than 5µA in quiescent mode.

In Fig. 2.4.4 the HV OCS is shown. The incoming DAC current is mirrored into the HV supply domain and is available with either polarity at the stimulation electrode. To achieve matched biphasic current pulses, low-voltage (LV) transistors are used for the mirrors in the HV domain, while HV transistors only shield the LV domain from overvoltage. The large number of electrodes prevents the use of standard ESD I/O pads, which would be about the required size of the stimulation pad cell. Thus, the large parasitic drain-bulk diodes of the HV output transistors in Fig. 2.4.4 are used as ESD diodes at each electrode. Further ESD and HV protection measures are implemented.

To prevent electrolysis the net dc-current must be kept below 10nA. Below this, only non-critical residual currents flow; above, the electrode potential accumulates to several 100mV and strong faradaic currents start to flow and electrolysis occurs. Such low dc current would require a biphasic current pulse matching of better than 10nA/992µA≈0.001% in the mirrors of the OCS. The large number of electrodes prevents external series capacitors for dc blocking, while discharge resistors between the stimulation electrodes only efficiently solve the problem if switched [3]; but HV (±15V) transmission gates are not available. Thus, an active charge balancer has been developed which zeros the voltage between the stimulation and the counter electrode after each stimulation cycle. A differential voltage measurement is done with no stimulation current flowing, which monitors the residual electrode charge. For this measurement a HV transconductance cell with source degeneration (Fig. 2.4.5) converts the small difference Ve-Vcm around the high common mode voltage (Vcm) into a current difference, mirrors it into the LV domain and converts it to a LV difference Vout, which is compared to a reference window. If this voltage exceeds a window of ±50mV a charge packet of suitable polarity is applied. This is repeated until the electrode voltage is within the safe window. This prevents electrode potential accumulation and electrolysis cannot occur.

A chip with 9 stimulation cells was designed to prove the critical functions of ESD protection, charge balancing and the HV capability. The chip size is 4.4×4.9mm² (Fig. 2.4.3). ESD tests at the electrodes show robust behaviour up to 2kV HBM. A measured HV output stimulation waveform is given in Fig. 2.4.6. Due to an experimentally imbalanced pulse, the charge balancer is activated and applies 2 short pulses and balances the electrode. Currently, a complete retinal stimulator chip is being fabricated, which includes all global functions and 116 stimulation pad cells. These are now modified in order to handle 2 output electrodes. Thus, a total of 232 stimulation sites are provided (Fig. 2.4.7).

References:

[1] W. Liu et al., "Retinal Prosthesis," *ISSCC Dig. of Tech. Papers*, pp. 218-219, Feb., 2004.
[2] Jun Ohta et al., "Retinal Prosthesis Device Based on Pulse-Frequency-Modulation," *IEEE Symp. Circ. Syst.*, pp. 2923-2926, May, 2005.
[3] W. Liu et al., "A Neuro-Stimulus Chip with Telemetry Unit for Retinal Prosthetic Device," *IEEE J. Solid State Circuits*, vol. 35, no. 10, pp. 1487-1497, Oct., 2000.
[4] M. Ortmanns et al., "Apparatus for Steering of Electrical Charge on Stimulation Electrodes," Pat. Appl. DE102004059973.4-54, 2004.

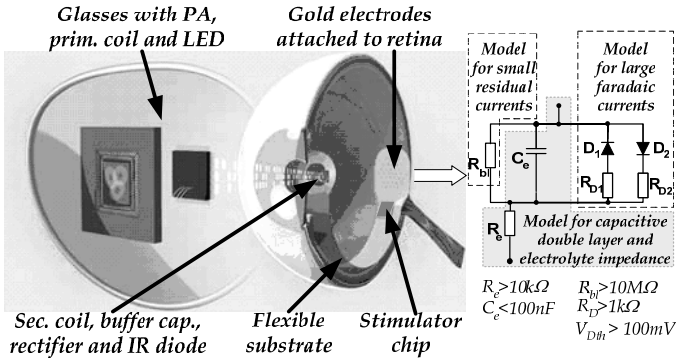

Figure 2.4.1: Epiretinal stimulator system and (basic) electrode model.

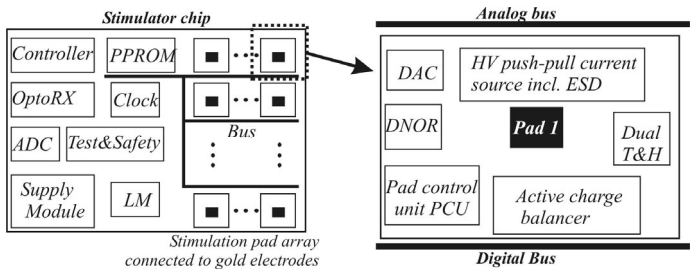

Figure 2.4.2: Block diagrams of the toplevel system and the distributed stimulation pads.

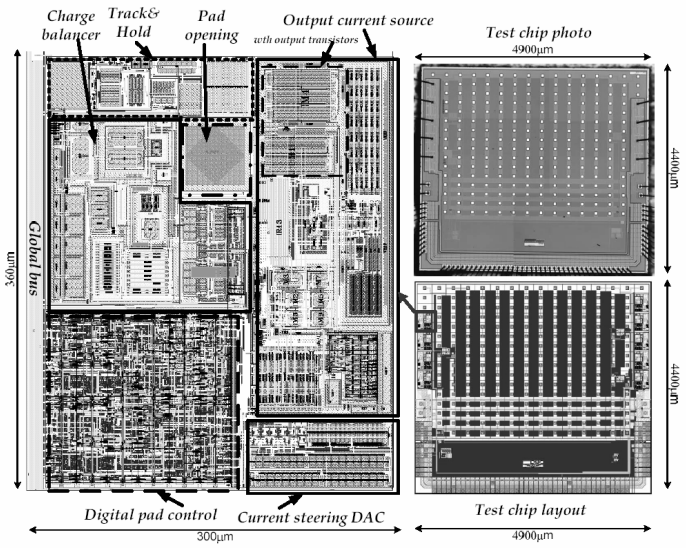

Figure 2.4.3: Floorplan and chip micrograph of pad cell and test chip.

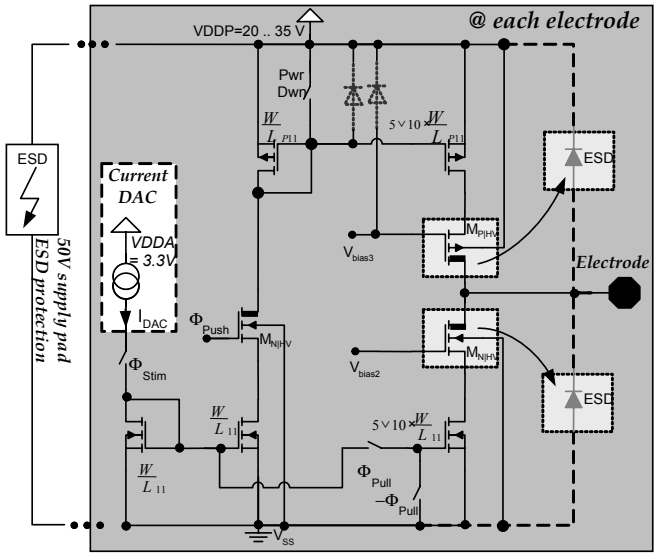

Figure 2.4.4: Output current source.

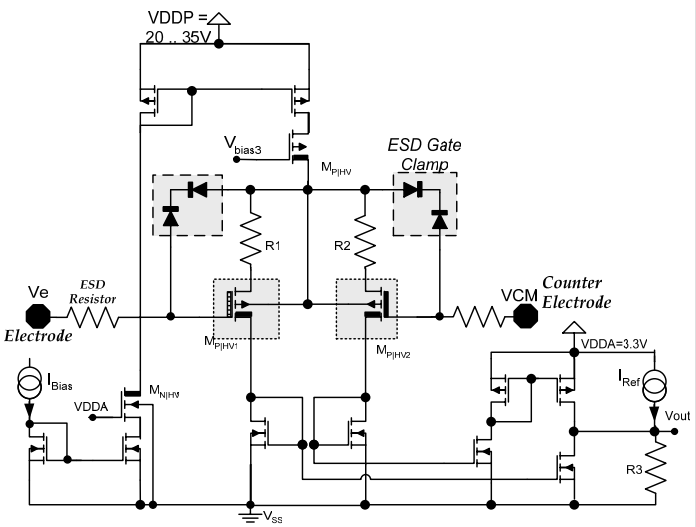

Figure 2.4.5: Charge balancer input stage.

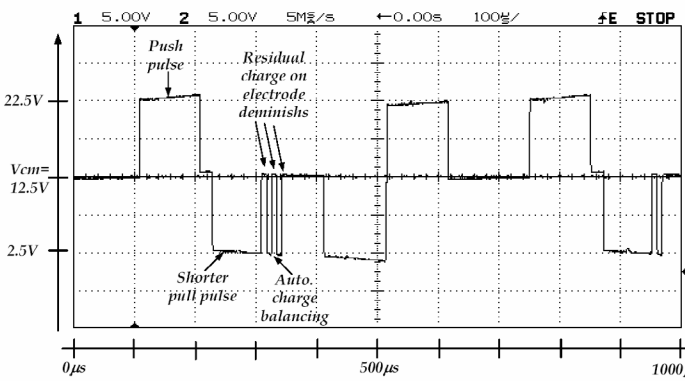

Figure 2.4.6: Measured stimulation waveform: 1mA into 10kΩ +100nF.

Continued on Page 636

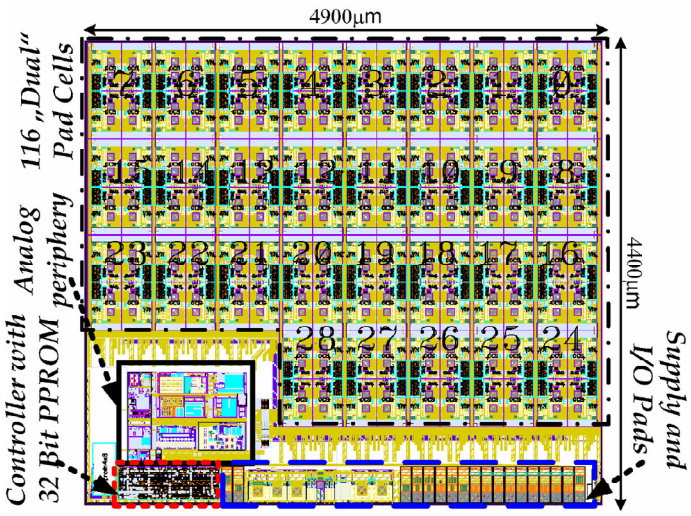

Figure 2.4.7: Chip layout of the retinal stimulator chip.

